Power Transformer Loss Measurement

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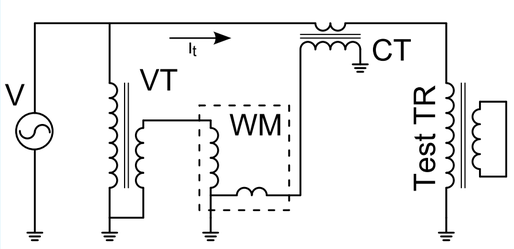
Background

- EU Ecodesign Directive requirements per 1 July 2015 on efficiency
- Similar requirements in IEC 60076-20 and IEEE C57.123-2010
- Customers: fines for excess loss 10 k€/kW

Transformer Loss Measurement System (TLMS)

Manufacturers of Power Transformers use commercially available TLMS for measurement of no-load and load-losses of their transformers

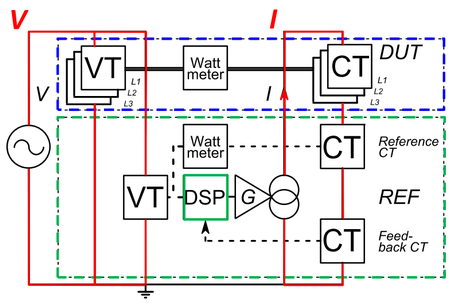


Three main components

- CT (5 kA)
- VT (100 kV)
- Watt meter

TLM calibration

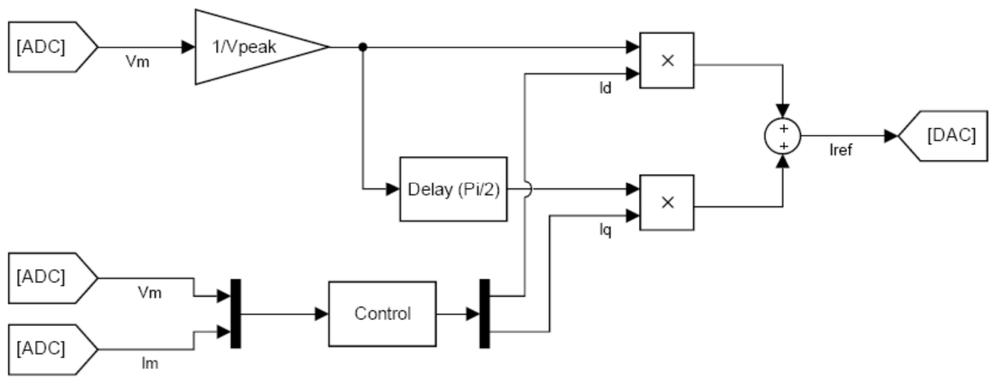
Approach to calibration: For given voltage reference (given on site), generate required P & Q set points for calibration through generating appropriate current reference!



Two Designs solutions

To solve the problem of digital implementation of accurate current reference generation, VSL and TU Delft have taken two different approaches with the aim to compare their effectiveness.

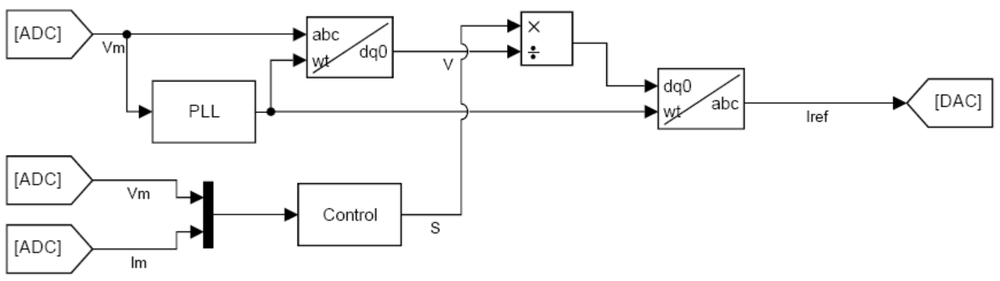
1. Orthogonal Signal System (VSL)*



- High-speed, low-accuracy (16 bit) loop to minimize propagation delay
- Low-speed, high-accuracy (24 bit) for feeding controller
- Various methods to generate quadrature signal (e.g. tr. Delay)
- ***Already implemented in hardware***

2. Synchronous Reference Frame (TU Delft)*

(Currently in design phase)



- Synchronize to input voltage using Phase Locked Loop
- Perform necessary calculations in d-q (rotating) reference frame
- Transform back in stationary reference frame
- Critical component – Phase Locked Loop (PLL)
- ***Currently in design phase***

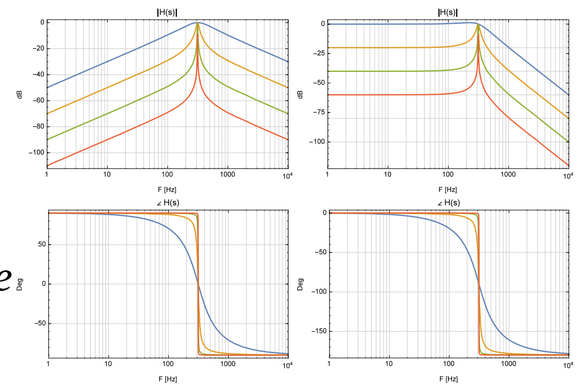
* The voltage transformer (VT), current transformer (CT) and other external equipment is omitted for simplicyt

Synchronous Reference Frame Generation

Generate a synchronous reference frame using a digital PLL

- **Key challenge - phase accuracy** (e.x. to achieve 3% accuracy of generated power reference at 0.01 power factor, the required phase accuracy is 300 μrad
- Several PLL circuits are investigated
  - ***Inverse-Park PLL*** –IParkPLL -(*most ubiquitous PLL used in Power Electronics Control)*
  - ***Enhanced PLL*** – EPLL - (*solves the problem of amplitude-dependet-gain present at IParkPLL)*
  - ***Second-Order Generalized Integrator PLL*** – SOGIPLL - *Orthogonal Signal is generated using a second order generalized integrator.*
  - ***Kalman-Filter based PLL*** – KFPLL – *orthogonal signal iz generated by applying Kalman Filter to a discrete Model of SOGI*

Detailed analysis revealed that all PLL offer similar performance in terms of harmonic rejection and dynamic response!

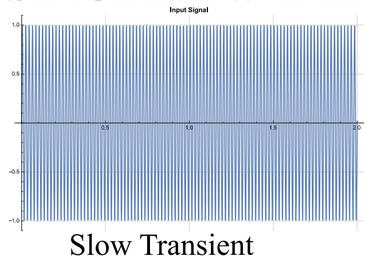


SOGI transfer functions

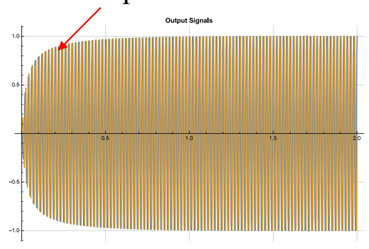
Summary of Current work and future plans

Current status

- Several PLL models investigated and their performance assessed and compared
- Simplified dynamic models of the system implemented in SIMULINK with initial simulation results

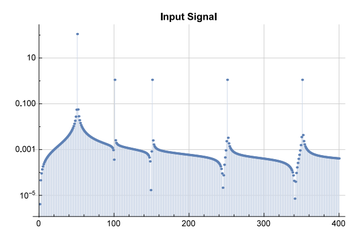


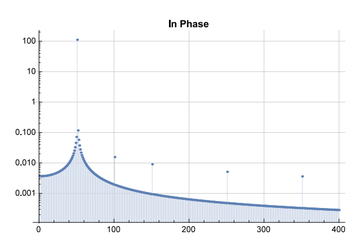
Slow Transient Response



High Penalty on Transient response.!

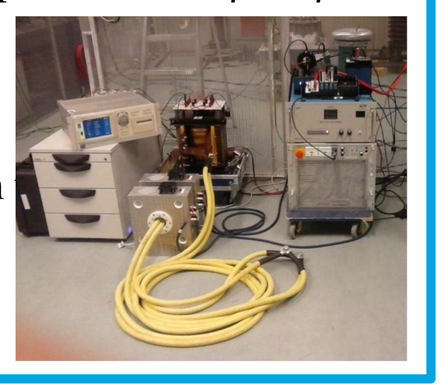
Tradeoff between harmonic suppression and transient response.





Future Plans

- Sensitivity analysis
- Effects of quantization and word size on accuracy and stability of the system
- Effects of harmonics
  - *Effects of power transfer at the frequency of harmonics* – given sufficiently large attenuation of the PLL at harmonics frequency, this effect will most likely be negligible.
  - *Influence of higher harmonics to the phase error of the first harmonics* (based on preliminary analysis, this effect will have to be addressed)
- Asses limitations of the system based on previous analysis
- Implement the proposed method on hardware



More Information

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DCE&S DC systems, Energy conversion & Storage

VSL