A Reference Merging Unit and Calibration Setup for Sampled Values over Ethernet

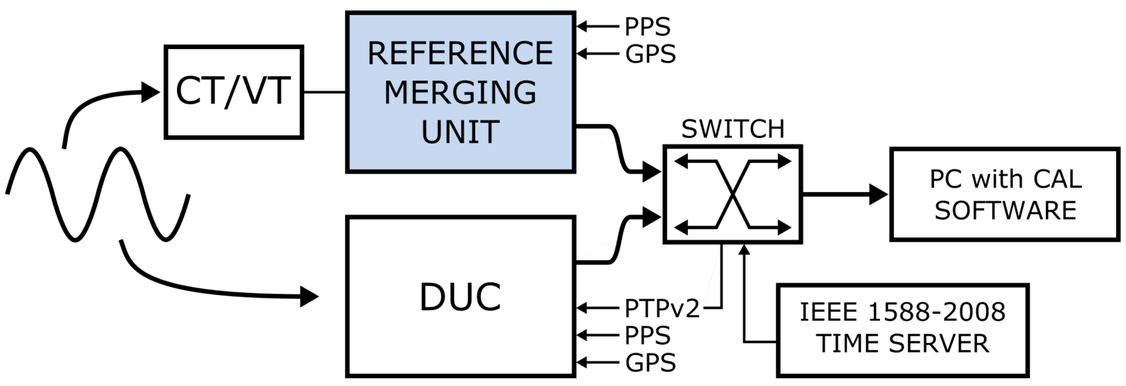
Tapio Lehtonen • Jari Hällström
VTT Technical Research Centre of Finland Ltd, Centre for Metrology MIKES

Motivation for the work

Modern electricity substations are migrating from vendor-specific standards for control and measurements into a universal, interoperable digital environment. A globally accepted standard, IEC 61850, defines among other things transfer of real-time substation events and sampled measurements over Ethernet. The latter is used for transmitting time-domain measurement data for protection and power quality use within a substation. Devices, which gather analog sensor data and convert it to digital format are called merging units Needless to say, traceable calibration for merging unit measurement data is needed to guarantee true interoperability.

Calibration method

The calibration is based on creating a reference sample stream as defined in implementation guideline IEC 61850-9-2 LE and comparing it to the stream generated by the device under calibration (DUC). Both devices measure the same input quantities and traceability for the DUC is established if the reference stream can be said to be traceable.

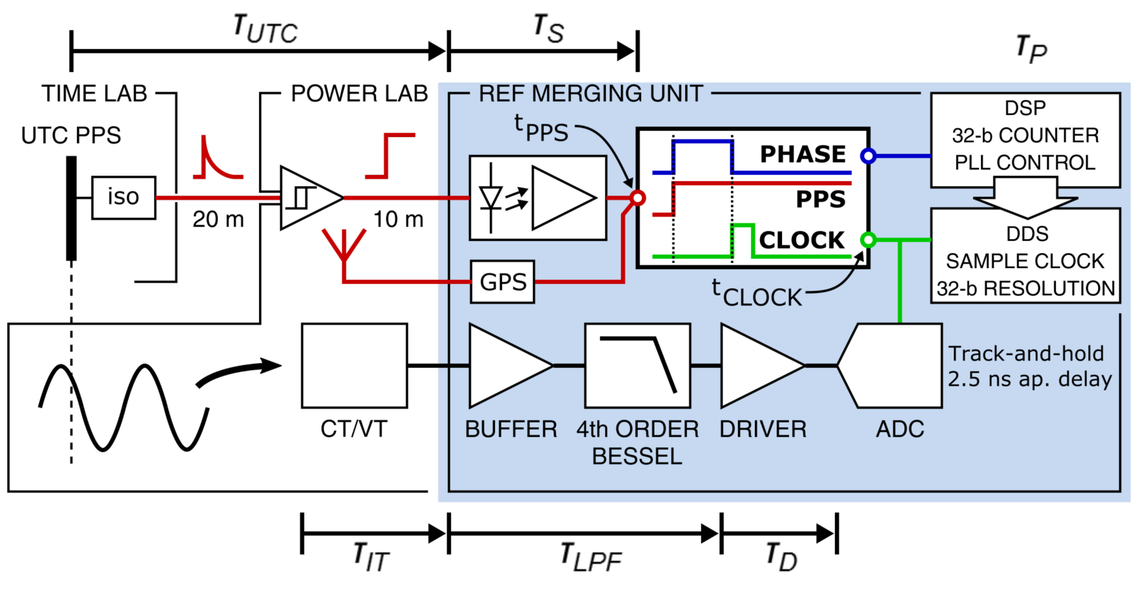


ABOVE: Block diagram of the calibration setup for IEC 61850-9-2 LE devices.

Reference merging unit traceability

Calibrating the signal gain for the reference stream can be done by calibrating all individual components, i.e. transducers and measurement device input. Since IEC 61850 requires for phase information to be referenced to global clock, often UTC, time delays within the signal chain need to be understood. This include reference timing and signal chain delays. Sample clock is adjusted so that the stream holds the true phase of measured signal vs. UTC reference. The required delay is

$$PHASE = t_{CLOCK} - t_{PPS} = \tau_{IT} + \tau_{PLPF} + \tau_D + \tau_P - \tau_{UTC} - \tau_S$$



ABOVE: Block diagram of the reference merging unit signal chain.

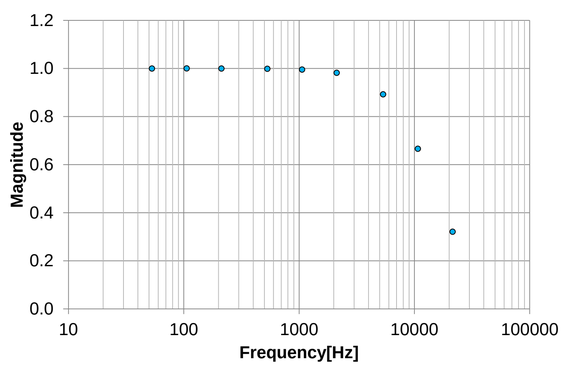
Reference merging unit

The reference digitizer is a custom six channel digitizer built around a digital signal processor (DSP) (CPEM 2014). The identical, floating input channels have internal buried Zener full-scale references, 18-bit SAR ADCs and a low-drift signal chain. Ranged low-pass filters can be selected if needed. Internal direct digital synthesis (DDS) based sample clock provides synchronized sampling for different modes of operation.

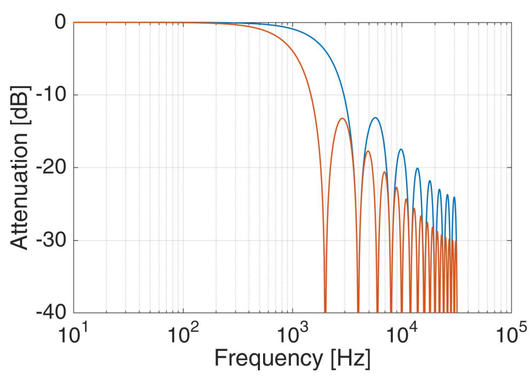
ABOVE: Reference merging unit.

Operation with 80 samples / cycle (MSVCB01)

IEC 61850-9-2 defines a sample rate of 80 samples per cycle for protection purposes, i.e. 4000 S/s for a 50 Hz nominal mains frequency. Measurement is oversampled at 16x rate (64 kS/s) for a relaxed anti-alias filter specification. A fourth-order 10 kHz low pass filter with a phase delay τ_{LPF} = 21.6 µs is used. Further digital filtering is required before downsampling. Digital filter delay τ_P is compensated by software.



ABOVE: Measured anti-alias filter amplitude response



ABOVE: Decimation filter responses 16-tap (blue) and 32-tap (red) moving average

Uncertainty budget

Total expanded uncertainty of the calibration setup for signal gain is 100 µV/V. Timing uncertainty contribution is summarized in the table below. Delay is given in nanoseconds and micro radians assuming a 50-Hz input signal.

Item	Symbol	Delay [µs]	Unc. [ns]	Unc. [µrad]	Comment
UTC	τ_{UTC}	cable	12	3.8	GPS, measured
Sampling	τ_S	0.1	15	4.7	PLL jitter
Anti-alias	τ_{LPF}	21.6	5	1.6	
Driver	τ_D	0.18	5	1.6	
Processing	τ_P	117	0	0	16-tap FIR
TOTAL reference MU		138.8-cable	20	6.4	

Contacts

Tapio Lehtonen
Tel. +358 50 511 0037
tapio.lehtonen@vtt.fi

Jari Hällström
Tel. +358 50 382 2127
jari.hallstrom@vtt.fi